REMARKS

Claims 4-83 are pending in this application. Claims 4-7, 9, 29, 36-42, 53, and 82-83 have been rejected. Claims 8, 10-28, 30-35, 43-52, and 54-81 have been allowed. Claim 83 has been cancelled without prejudice.

Claims 4-7, 9, 29, 36-39, 53, and 82-83 have been rejected under 35 U.S.C. § 102(e) as being anticipated by *Tsen* (U.S. Patent No. 5,936,906). This rejection is respectfully traversed.

Tsen at best merely discloses a primary cells array 100 that includes flash cells that store multilevel digital data. A word decoder 102 selects flash cells using word lines WL. A bitline decoder 104 selects bitlines BL connected to the flash cells. ('906 patent, col. 2, l. 60-col 3, l. 5.) "[A] reference cells array 110 is electrically coupled to the primary cells array 100 via the word lines [WL] for sharing the word lines [WL]." ('906 patent, col. 3, lns. 6-8.) The reference latch cells are set at threshold voltages by applying reference signals to the corresponding word line that is selected by the word line decoder 102. ('906 patent, col. 3, l. 66-col. 4, l. 16.) During reads from the memory cells, the current from the read memory cell is compared in the sense amplifier 120 to the reference currents stored in the reference cells array 110. ('906 patent, col. 4, lns. 38-59.)

Claim 4 recites in pertinent part a plurality of multidimensional memory arrays.

Tsen does not disclose or even suggest multidimensional memory arrays. Instead, Tsen discloses a single memory array and a reference array. In contrast, claim 4 recites a plurality of multidimensional memory arrays and a reference array. The Office Action asserts that multilevel digital data in the memory cell is a multidimensional memory array. As recited in claim 4, multidimensional does not refer to multilevel digital data. Claim 4 separately recites "each memory cell is configurable to store one of 2^N values wherein N is 2 or greater". The memory arrays are multidimensional, which is in addition to the memory cell storing one of 2^N values. As an illustrative embodiment, the memory arrays may be multidimensional as shown in Figures 2A and 3A of the application.

Lacking the disclosure of this claim feature, *Tsen* cannot render claim 4 unpatentable. Because claims 5-7, 36-42, and 53 depend, directly or indirectly, on claim 4, for similar reasons claims 5-7, 36-42 and 53 are not rendered unpatentable by *Tsen*. Therefore, it is respectfully submitted that claims 4-7, 36, 42 and 53 are patentable over the references of record.

Claim 82 recites in pertinent part a plurality of segmented memory arrays. *Tsen* discloses an array of memory cells, but does not disclose or even suggest segmented memory arrays as recited in claim 82. The Office Action does not state where *Tsen* discloses segmented memory arrays as recited in claim 82. The Examiner is respectfully reminded of the provisions of 37 CFR §1.104(c)(2) (cited in MPEP §706):

> "When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified."

Further, as stated in MPEP §707:

> "In accordance with the patent statute, 'Whenever, on examination, any claim for a patent is rejected or any objection . . . made,' notification of the reasons for rejection and/or objection together with such information and references as may be useful in judging the propriety of continuing the prosecution (35 U.S.C. 132) should be given."

Because *Tsen* does not disclose or even suggest segmented memory arrays as recited in claim 82, *Tsen* cannot render claim 82 unpatentable.

Therefore, it is respectfully submitted that claim 82 is patentable over the references of record.

Claim 83 has been cancelled without prejudice.

Claims 40-42 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Tsen* in view of *Banks* (U.S. Patent No. 6,602,614). This rejection is respectfully traversed.

As described above, *Tsen* does not disclose multidimensional memory arrays. *Banks* at best merely discloses a multibit per cell electrically alterable non-volatile memory system 100 that includes an MxN array of non-volatile cells. Word lines 104 connect the memory cells. Bitlines 106 connect columns of memory cells. The output of sense amplifiers 112 coupled to the bitlines and a reference voltage detect a voltage. A decode/encode circuit 114 decodes the data bits which are latched in an input/output, N-bit latch/buffer 116. ('614 patent, Fig. 5, col. 8, l. 43-col. 9, l. 7.) The array of *Banks* is not a multidimensional memory array, but a single array.

Claims 40-42 depend directly or indirectly on claim 4. Neither *Tsen* nor *Banks*, either individually or in combination, disclose or even suggest a plurality of multidimensional memory

arrays as recited in claim 4, or in claims 40-42, and thus cannot render claims 40-42 unpatentable.

Therefore, it is respectfully submitted that claims 40-42 are patentable over the references of record.

The allowance of claim 8, 10-28, 30-35, 43-52, and 54-81 is noted.

It is submitted that claims 4-7, 9, 29, 36-42, and 82 are allowable, and allowance and issuance of this application is respectfully requested.

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Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned APPENDIX – MARKINGS TO SHOW CHANGES MADE.

Please charge any additional fees, including any fees necessary for extensions of time, or credit overpayment to Deposit Account No. **07-1896, referencing 2102397-991720.**

Dated: November 27, 2002

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